DHRUVA GHAI

Pro-Chancellor
Professor, Electronics and Communication Engineering
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PROFILE

- Versatile Professional with 15 years of combined experience in the Academia as well as Industry.
- International industry and teaching experience with strong research skills.

EDUCATIONAL BACKGROUND

Institute	Major	Degree	Year
University of North Texas, TX, USA	Computer Science and Engineering	Ph.D.	2009
Rajiv Gandhi Technological University, India	Microelectronics and VLSI	M.Tech.	2006
University of Pune, India	Electronics and Communication	B.E.	2003
Indian Institute of Management (IIM), Indore	General Management	E.P.G.P.	2017

PROFESSIONAL EXPERIENCE

Pro-Chancellor Oct 2024- Current
Oriental University, Opp.Revati Range Gate No.1, Sanwer Road,Jakhya, Indore-453555, Madhya Pradesh, India

- Provide leadership in academics and administration, and act as a leader of the governing authority to ensure efficient operations and proper conduct within the University.
- Develop and implement academic enhancement and faculty development programs (FDPs) for students and staff, as well as developing new policies related to research and faculty incentives.
- Foster collaboration with external entities like HCLTech to introduce skill development programs and explore opportunities for international collaborations.
- Communicate with accreditation bodies such as NCTE, BCI, PCI, and ICAR, and ensure sufficient resources and direction are available to establish and maintain a culture of compliance.
- Plan the budget schedule and allocate resources for college and community-related activities.
- Recruit high-calibre faculty and maintain high standards of competence in teaching methodologies through professional development activities.
- Prioritize students' interests and ensuring their concerns are addressed efficiently, treating them as valued "customers" who deserve the best facilities and support.

Pro-Vice-Chancellor July 2018- Oct 2024
Oriental University, Opp.Revati Range Gate No.1, Sanwer Road,Jakhya, Indore-453555, Madhya Pradesh, India

- Support the Vice-Chancellor in the leadership of the university.
- Provide input for strategic planning, policy development, implementation, review and monitoring.
- Lead the efforts for process improvements in the university.
- Communicate and liaison with accreditation bodies such as NCTE, BCI, PCI and ICAR.
- Recruit and appoint high calibre faculty to the university.
- Develop and improve policies of the university involving research, incentives for faculties.
- Sign and execute MoUs on behalf of the university.
- Act as Officiating Vice-Chancellor in the Vice-Chancellor's absence.

Professor and Dean, Engineering and Technology May 2012- July 2018
Oriental University, Opp.Revati Range Gate No.1, Sanwer Road,Jakhya, Indore-453555, Madhya Pradesh, India

- Provide vision and dynamic leadership to the School of Engineering; lead and represent the academic departments within the School.
- Oversee the establishment and milestone achievement of the Microsoft Innovation Center (MIC) under the Microsoft-Edvantage program at Oriental University.

- Oversee the university website development and maintenance. Handle the digital marketing at Oriental University.
- Handle the task of maintaining high standards of competence in teaching methodologies through professional/faculty development activities.
- Oversee the ERP implementation in an effort to make the University functioning paperless. Assign the tasks of planning and designing various projects based on electronics/software.
- Lab/EDA (electronic design automation) using free forms of SPICE tools/layout tools and Matlab/ Simulink.
- Chaired and conducted International conference (http://ieee-inis.org) at Indore.

Data Integration Developer July 2011- April 2012
Viverae Inc., 10670 N. Central Expressway Suite 700, Dallas, Texas 75231

- Interfaced with the business analyst to convert business requirements into ETL processes.
- Automated medical claims data processing.
- Increased client satisfaction by ensuring timely delivery of incentive reports through automation.

ETL Developer August 2010- June 2011
Novedea Systems Inc., 1750 N Collins Blvd, Suite 212, Richardson, TX 75080

- Worked with development teams to review and develop data models and database designs to meet functionality deliverables in the project document.
- Evaluated new ETL software for SME market.
- Provided training to new members in the team to get them upto speed on new software quickly and developing strong client facing skills.

Analog Design Engineer October 2009- July 2010
nanoDragon LLC, 3103 Brookview Dr., Corinth, TX 76210

- Involved in the design of an Optical Sensor ASIC using xfab XC06 (0.6m) technology.

Adjunct Faculty Fall 2009
University of North Texas, Department of Computer Science and Engineering, 3940 N. Elm, F201, Denton, TX 76207-7102

- Taught Computer Science and Engineering related courses like Computer Organization and Reconfigurable Logic.
- Prepared course syllabi, lesson plans, teaching aids, exams and other instructional materials.
- Taught VHDL/Verilog programming to students.
- Taught Assembly Language Programming for MIPS processor.
- Taught ALU design for MIPS processor using VHDL.
- Conducted FPGA programming labs for students.

PROFESSIONAL AFFILIATIONS AND ACTIVITIES

- 2019 UNT CSE Recent Alumni Award.
- Senior Member, IEEE.
- Member, IEEE-Computer Society.
- Member, IEEE-Consumer Electronics Society.
- Fellow, IETE, India.
- General Chair, IEEE International Symposium on Nanoelectronic and Information Systems (IEEE-iNIS) 2017, Indore, India.
- Vice-Chair, IEEE International Symposium on Nanoelectronic and Information Systems (IEEE-iNIS) 2015, Indore, India.
- Technical Program Committee, ISQED.
- Program Committee Member, ISVLSI.
- Technical Program Committee, GLSVLSI.
- Reviewer: IEEE Transactions on Semiconductor Manufacturing, IEEE Transactions on VLSI, Elsevier Microelectronics Journal, Integration, the VLSI Journal (Awarded Outstanding Reviewer status in November 2017), Springer Analog and Signal processing Journal, ISQED 2013, ICCD 2013, ISQED 2014, ISVLSI 2014, VDAT 2014, GLSVLSI 2014.
- Alumni, Management Development Programme on Leadership Communication, I.I.M. Indore.

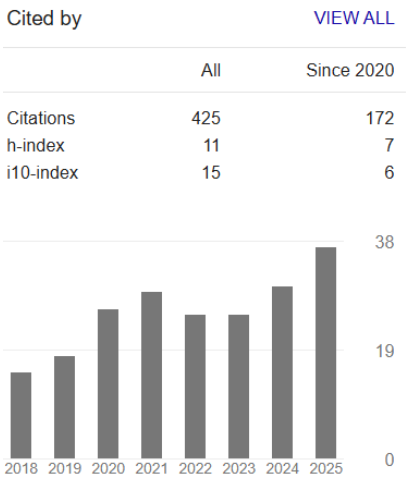

Figure 1: Citations received by my articles as calculated by the Google Scholar.

- Alumni, Management Development Programme on Train the Trainer Programme, I.I.M. Indore.
- Runner up in Bulls and Bears competition - Company Financial Analysis held at I.I.M. Indore.
- Member, Academic Committee and Corporate Interaction Committee, EPGP program, I.I.M. Indore.
- Completed the "Advanced Program in Analytics for Business Excellence" from University of Texas at Austin, McCombs School of Business, USA.
- Achieved statement of accomplishment with distinction in a MOOC conducted by Dr. James V. Green of University of Maryland, College Park on "Developing Innovative Ideas for New Companies" on coursera platform.
- Achieved statement of accomplishment in a MOOC conducted by Dr. Tobias Kretschmer of Ludwig Maximilian University (LMU) of Munich on "Competitive Strategy" on coursera platform.
- Achieved statement of accomplishment in a MOOC titled "Introduction to Search Engine Optimization" by University of California, Davis on Coursera. Certificate earned on February 29, 2016
- Microsoft Technology Associate, Database Fundamentals.
- Microsoft Certified Professional.

PhD Dissertations Supervised

1. G. Vaseer, Ph.D.(Computer Science), Dissertation: "Novel Intrusion Detection and Prevention Techniques for Mobile Ad Hoc Networks", Department of Computer Science and Engineering, Oriental University Indore, July 2019, Major Professor.

PUBLICATIONS

1. S. Vishwakarma, G. Raut, S. Jaiswal, S. K. Vishvakarma, and D. Ghai, "A Precision-Aware Neuron Engine for DNN Accelerators", in Springer Nature Computer Science, vol. 5, no. 5, pp. 494, April 2024.
2. S. Vishwakarma, G. Raut, N. S. Dhakad, S. K. Vishvakarma, and D. Ghai, "A Configurable Activation Function for Variable Bit-Precision DNN Hardware Accelerators", in IFIP International Internet of Things Conference, pp. 433-441, 2023.
3. V. P. Yanambaka, S. P. Mohanty, E. Kougianos, and D. Ghai, "Memristor Devices and Memristor-based Circuits", in Advanced Technologies for Next Generation Integrated Circuits, Edited by A. Srivastava and S. P. Mohanty, The Institute of Engineering and Technology (IET), 2020, ISBN-10: 1785616641, ISBN-13: 978-1785616648.
4. D. Ghai, "Computing in Geographic Information Systems: Book Review ", in IEEE Consumer Electronics Magazine, vol. 8, no. 4, pp. 80-80, July 2019.

5. G. Vaseer, G. Ghai and D. Ghai, "Novel Intrusion Detection and Prevention for Mobile Ad Hoc Networks: A Single- and Multiattack Case Study", in IEEE Consumer Electronics Magazine, vol. 8, no. 3, pp. 35-39, May 2019.
6. G. Vaseer, G. Ghai, D. Ghai and P. S. Patheja, "A Neighbor Trust-Based Mechanism to Protect Mobile Networks," in IEEE Potentials, vol. 38, no. 1, pp. 20-25, Jan.-Feb. 2019.
7. V. P. Yanambaka, S. P. Mohanty, E. Kougianos, D. Ghai, and G. Ghai, "Process Variation Analysis and Optimization of a FinFET based VCO", IEEE Transactions on Semiconductor Manufacturing (TSM), Vol. 30, No. 02, May 2017, pp. 126-134.
8. V. P. Yanambaka, S. P. Mohanty, E. Kougianos, and D. Ghai, "Nanoscale High-K/Metal-Gate CMOS and FinFET based Logic Libraries", in Nano-CMOS and Post-CMOS Electronics: Devices and Modelling, Edited by S. P. Mohanty and A. Srivastava, The Institute of Engineering and Technology (IET), 2016, ISBN-10: 1849199973, ISBN-13: 978-1849199971.
9. D. Ghai, S. P. Mohanty, and G. Thakral, "Fast Optimization of Nano-CMOS Voltage-Controlled Oscillator using Polynomial Regression and Genetic Algorithm", Elsevier Microelectronics Journal (MEJ), Volume 44, Issue 8, August 2013, pp. 631–641.
10. D. Ghai, S. P. Mohanty, and E. Kougianos, "A Variability Tolerant System-on-Chip Ready Nano-CMOS Analog-to-Digital Converter (ADC)", Taylor and Francis International Journal of Electronics (IJE), Vol. 97, No. 4, April 2010, pp. 421–440.
11. D. Ghai, S. P. Mohanty, and E. Kougianos, "Design of Parasitic and Process-Variation Aware Nano-CMOS RF Circuits: A VCO Case Study", in IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Vol. 17, No. 9, September 2009, pp. 1339-1342.
12. D. Ghai, S. P. Mohanty, G. Thakral, and O. Okobiah, "Variability-Aware DG FinFET-based Current Mirrors", in Proceedings of the 23rd ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), pp. 347-352, 2014.
13. D. Ghai, S. P. Mohanty, and G. Thakral, "Comparative Analysis of Double Gate FinFET Configurations for Analog Circuit Design", in Proceedings of the 56th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 809-812, 2013.
14. D. Ghai, S. P. Mohanty, and G. Thakral, "Double Gate FinFET based Mixed-Signal Design: A VCO Case Study", in Proceedings of the 56th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 177-180, 2013.
15. D. Ghai, S. P. Mohanty, and G. Thakral, "Fast Analog Design Optimization using Regression based Modeling and Genetic Algorithm: A Nano-CMOS VCO Case Study", in Proceedings of the 14th IEEE International Symposium on Quality Electronic Design (ISQED), pp. 422–427, 2013.
16. S. P. Mohanty, D. Ghai, and E. Kougianos, "A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-VTh Nano-CMOS VCO", in Proceedings of the 23rd IEEE International Conference on VLSI Design (VLSID), pp. 99-104, 2010.
17. G. Thakral, S. P. Mohanty, D. Ghai, and D. K. Pradhan, "A Combined DOE-ILP Based Power and Read Stability Optimization in Nano-CMOS SRAM", in Proceedings of the 23rd IEEE International Conference on VLSI Design (VLSID), pp. 45-50, 2010.
18. G. Thakral, S. P. Mohanty, D. Ghai, and D. K. Pradhan, "A DOE-ILP Assisted Conjugate-Gradient Approach for Power and Stability Optimization in High-κ/Metal-Gate SRAM", in Proceedings of the 20th ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), pp. 323-328, 2010.
19. G. Thakral, S. P. Mohanty, D. Ghai, and D. K. Pradhan, "P3 (Power-Performance-Process) Optimization of Nano-CMOS SRAM using Statistical DOE-ILP", in Proceedings of the 11th IEEE International Symposium on Quality Electronic Design (ISQED), pp. 176-183, 2010.
20. D. Ghai, S. P. Mohanty, and E. Kougianos, "Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO", in Proceedings of the 19th ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), pp. 303-308, 2009.
21. D. Ghai, S. P. Mohanty, and E. Kougianos, "Variability-Aware Optimization of Nano-CMOS Active Pixel Sensors using Design and Analysis of Monte Carlo Experiments", accepted in

Proceedings of the 10th IEEE International Symposium on Quality Electronic Design (ISQED), 2009.

22. S. P. Mohanty, D. Ghai, E. Kougianos, and P. Patra, "A Combined Packet Classifier and Scheduler Towards Net-Centric Multimedia Processor Design", in Proceedings of the 27th IEEE International Conference on Consumer Electronics (ICCE), pp. 11-12, 2009.
23. D. Ghai, S. P. Mohanty, E. Kougianos, and P. Patra, "A PVT Aware Accurate Statistical Logic Library for High-K Metal-Gate Nano-CMOS", in Proceedings of the 10th IEEE International Symposium on Quality Electronic Design (ISQED), pp. 47-54, 2009.
24. S. P. Mohanty, D. Ghai, E. Kougianos, and B. Joshi, "A Universal Level Converter Towards the Realization of Energy Efficient Implantable Drug Delivery Nano-Electro-Mechanical-Systems", in Proceedings of the 10th IEEE International Symposium on Quality Electronic Design (ISQED), pp. 673-679, 2009.
25. D. Ghai, S. P. Mohanty, and E. Kougianos, "A Process and Supply Variation Tolerant Nano-CMOS Low Voltage, High Speed, A/D Converter for System-on-Chip", in Proceedings of the 18th ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI), 2008, pp. 47-52.
26. D. Ghai, S. P. Mohanty, and E. Kougianos, "A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-VDD SoCs", in Proceedings of the 9th IEEE International Symposium on Quality Electronic Design (ISQED), 2008, pp. 257-260.
27. D. Ghai, S. P. Mohanty, and E. Kougianos, "Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design", in Proceedings of the 9th IEEE International Symposium on Quality Electronic Design (ISQED), 2008, pp. 330-333.
28. D. Ghai, S. P. Mohanty, and E. Kougianos, "A 45nm Flash Analog to Digital Converter for Low Voltage High Speed System on Chips", in Proceedings of the 13th NASA Symposium on VLSI Design, 2007.
29. S. P. Mohanty, E. Kougianos, D. Ghai, and P. Patra, "Interdependency Study of Process and Design Parameter Scaling for Power Optimization of Nano-CMOS Circuits under Process Variation", in Proceedings of the 16th ACM/IEEE International Workshop on Logic and Synthesis (IWLS), pp. 207-213, 2007.